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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/727,362	12/04/2003	Joseph R. Nicolaisen	016295.1508 (DC-05570)	6951
23640	7590	06/26/2006	EXAMINER	
BAKER BOTTS, LLP			VIGUSHIN, JOHN B	
910 LOUISIANA			ART UNIT	
HOUSTON, TX 77002-4995			PAPER NUMBER	
			2841	

DATE MAILED: 06/26/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/727,362

Applicant(s)

NICOLAISEN, JOSEPH R.

Examiner

John B. Vigushin

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 07 April 2006.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 8-20 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 8, 12-14 and 18-20 is/are rejected.
- 7) ☒ Claim(s) 9-11 and 15-17 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 04 December 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

1. The present Office Action is responsive to Applicant's Amendment filed April 07, 2006. The Examiner acknowledges the amendments to Claims 8 and 14, and the cancellation of Claims 1-7 which were non-elected responsive to Examiner's Restriction requirement in the previous Office Action of January 10, 2006. Accordingly, Claims 8-20 remain pending in the instant amended Application.

References Based On Prior Art

2. The following references were relied upon for the rejections hereinbelow:

Kabumoto et al. (US 6,707,685 B2)† Davis et al. (US 5,206,074)

†Already made of record in Examiner's previous Office Action of January 10, 2006.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 8, 14 and 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Kabumoto et al. [Examiner's Note: For the rejections of Claims 8 and 14, below, in

Examiner's Note #2, Davis et al. is relied upon to show that the insulating layers of Kabumoto et al. are, in fact, enabled as "cores," as taught by Davis et al., in accordance with the practice of multiple reference rejections under 35 USC § 102 as explained in the MPEP § 2131.01, part I].

As to Claim 8, Kabumoto et al. discloses, in Fig. 4, a PCB 21 comprising: a first core 22c; a second core 22e; and an insulating material 22d having regions 29 of increased permittivity, the insulating material 22d operable to couple the first core 22c to the second core 22e—mechanically through the lamination process (col.26: 37-53) and electrically through the vias, not shown, between the signal/power/ground patterns 23b and 23d (col.13: 55-59)—and the regions 29 of increased permittivity (col.14: 5-14) disposed proximate to at least one hybrid power plane 24a,b (col.13: 32-65).

[Examiner's Note #1: the hybrid power plane 24 consists of the coplanar power layer pattern 24a and signal/power/ground patterns 23c on the top surface of hybrid power plane 24 and the coplanar ground layer 24b and signal/power/ground patterns 23d on the bottom surface of hybrid power plane 24 (col.13: 62-col.14: 4); the "hybrid" concept that so defines power plane 24 lies in the coplanar accommodation of power, signal and ground metallizations on each side of the power plane 24, which is more explicitly shown in Fig. 1E, which shows the top surface of layer 2d from Fig. 1A, similar to the embodiment of Fig. 4). Examiner's Note #2: Although Kabumoto et al. does not use the word "core" but refers to 22a,b,c,d,e as "insulating layers" stacked on top of each other (in particular, organic layers, col.13: 37-39; col.26: 10-21 and 37-53), such stacked (i.e., laminated) metallized organic layers are encompassed by the concept of laminated

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"cores," taught as cores 11, in Fig. 1 and col.5: 65-col.6: 10 in Davis et al. Accordingly, the Examiner considers the "insulating layers" 22a,b,c,d,e in the laminated package in Fig. 4 of Kabumoto et al. to be enabled as "cores" by the disclosure of cores in Davis et al.].

As to Claim 14, Kabumoto discloses a method for manufacturing a PCB 21 having at least a first core 22c and a second core 22e comprising: integrating an insulating material 29 having a first permittivity into at least a portion of a dielectric layer 22d having a second permittivity (col.14: 51-58; col.26: 58-col.27: 3; col.27: 13-20); and coupling the first and second cores 22c and 22e together about the dielectric layer 22d such that the insulating material integrated portions 29 of the dielectric layer 22d substantially align with a hybrid power delivery plane 24 (specifically, plane 24a and/or plane 24b) defined by at least a portion of the first and second cores 22c and 22e (col.13: 32-65). Examiner's Note #1: hybrid power plane 24 consists of the coplanar power layer 24a and signal/power/ground layers 23c on the top surface of hybrid power plane 24 and the coplanar ground layer 24b and signal/power/ground layers 23d on the bottom surface of hybrid power plane 24 (col.13: 62-col.14: 4); the "hybrid" concept that so defines power plane 24 lies in the coplanar accommodation of power, signal and ground metallizations on each side of the power plane 24, which is more explicitly shown in Fig. 1E, which shows the top surface of layer 2d from Fig. 1A, similar to the embodiment of Fig. 4). Examiner's Note #2: Although Kabumoto et al. does not use the word "core" but refers to 22a,b,c,d,e as "insulating layers" stacked on top of each other (in particular, organic layers, col.13: 37-39; col.26: 10-21 and 37-53), such stacked (i.e.,

laminated) metallized organic layers are encompassed by the concept of laminated "cores," taught as cores 11, in Fig. 1 and col.5: 65-col.6: 10 in Davis et al. Accordingly, the Examiner considers the "insulating layers" 22a,b,c,d,e in the laminated package in Fig. 4 of Kabumoto et al. to be enabled as "cores" by the disclosure of "cores" in Davis et al.].

As to Claim 18, Kabumoto et al. further discloses reprocessing the dielectric layer 22d to permit addition of an increased permittivity insulating material 29 therein (col.26: 58-col.27: 20).

As to Claim 19, Kabumoto et al. further discloses maintaining portions of the dielectric layer 22d substantially free from insulating material 29 where such areas substantially align with signal pathways 23d of a selected core 22e (Fig. 4).

As to Claim 20, Kabumoto et al. further discloses coupling a first panel 22c and second panel 22e together about the dielectric layer 22d such that the insulating material integrated portions 29 of the dielectric layer 22d substantially align with a power delivery plane (plane 24a or 24b) to be defined by at least a portion of the first and second panels 22c and 22e (Fig. 4; col.14: 51-58).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 12 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kabumoto et al.

A) As to Claim 12:

I. Kabumoto et al. further discloses a third core 22a and an additional insulating material 22b, the additional insulating material 22b operable to couple the first core 22c to the third core 22a (Fig. 4).

II. Kabumoto et al. does not teach regions of increased permittivity in the additional insulating material 22b but does teach a capacitance 25 (different in value from the capacitance 24) so that the first and second built-in capacitors 24 and 25 have mutually different resonant frequencies, as required, to minimize the composite impedance at an anti-resonance frequency occurring between the resonant frequencies of the built-in power plane capacitors 24, 25 (col.5: 10-33) in order to reduce switching noise (col.5: 34-42; col.14: 51-67). Kabumoto et al. further teaches that there may be three or more power plane capacitors of the type 24, 25 in the package 21 (col.27: 63-64).

III. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kabumoto et al. with more regions of high permittivity 29 located within the additional insulating material 22b to either increase the permittivity of the given material 22b between power/ground planes 25a,b or to create additional regions of high permittivity within additional insulating material 22b in order to optimize switching noise reduction in the package for meeting the particular requirements of an application by minimizing the composite impedance at an anti-

resonance frequency occurring between the resonant frequencies of the built-in capacitors, said resonant frequencies being controlled by the capacitance values of the capacitors which are determined, at least in part, by materially adjusting the regions of increased permittivity within the additional insulating material accordingly.

B) As to Claim 13:

I. Kabumoto et al. further discloses, in Fig. 4, at least two power planes 24 and 25, wherein power plane 24 is defined between core 22c and core 22e, and power plane 25 is defined between core 22c and core 22a; and a region of permittivity by insulating material 22b and a region of increased permittivity 29 disposed substantially within insulating material 22d of power plane 24, the two regions of permittivity having differing capacitance values (Fig. 4; col.14: 51-63) in order that the two capacitors having different resonance frequencies (col.14: 63-67).

II. Kabumoto et al. does not teach at least two regions of increased permittivity 29 disposed within respective power planes 24 and 25 but teaches one such region 29 within power plane 24 and the other region in power plane 25 comprising the same material as insulating material 22b which results in the two different capacitance values between planes 24a,b of power plane 24 and planes 25a,b of power plane 25.

III. However, Kabumoto et al. further teaches that there may be three or more power plane capacitors of the type 24, 25 in the package 21 (col.27: 63-64) and since these differing capacitances within power planes are so constructed with particular values relative to one another to minimize the composite impedance at an anti-resonance frequency occurring between the resonant frequencies of the built-in

capacitors (col.5: 10-33) in order to reduce switching noise (col.5: 34-42; col.14: 51-67), then it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Kabumoto et al. with at least two regions of high permittivity located within insulating material 22d and/or 22b by either increasing the permittivity of the given material 22b between power/ground planes 25a,b, or to create additional regions of high permittivity between power/ground planes within insulating material 22b and/or 22d in order to optimize switching noise reduction in the package for meeting the particular requirements of an application by minimizing the composite impedance at an anti-resonance frequency occurring between the resonant frequencies of the built-in capacitors, said resonant frequencies being controlled by the capacitance values of the capacitors which are determined, at least in part, by materially adjusting the regions of increased permittivity within the power layers built into a core insulating material accordingly.

Response to Arguments

7. Applicant's arguments, see Remarks on p.5 of Applicant's Amendment, filed April 07, 2006, with respect to the rejection(s) of claim(s) 8 and 14 under Lee et al. (US 2004/0118600 A1) have been fully considered and are persuasive. Therefore, the rejection has been withdrawn. However, upon consideration of Applicant's amended Claims 8 and 14, a new ground(s) of rejection is made in view of Kabumoto et al. (US 6,707,685 B2) in conjunction with Davis et al. (US 5,206,074).

Allowable Subject Matter

8. Claims 9-11 and 15-17 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

9. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a) Kanazawa et al. (US 5,059,407) discloses a hybrid power plane (Fig. 4 and 26; col.6: 11-32; col.9: 10-12).

b) Conn et al. (US 5,418,690) discloses a hybrid power plane (Fig. 2 and col.3: 37-43: core 18 comprises hybrid of power planes 22, 23 and signal patterns 24; core 19 comprises hybrid of power planes 25, 26 and signal patterns 27).

c) Nakao et al. (US 5,926,377) discloses second core 24 that couples first core 21 and third core 27 with high permittivity regions 40 within power plane 23, 25 defined between first core 21 and third core 27 (see Fig. 15b in conjunction with Fig. 2a, the embodiment of Fig. 15b being a variant of the Fig. 2a embodiment; col.4: 30-35 and col.7: 55-col.8: 9). Power layer 23 and ground layer 25 are uniformly power/ground layers; not hybrid layers, wherein power and/or ground layers also include coplanar metallization having a different function from power and/or ground, respectively.

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10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

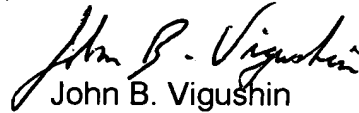
A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to John B. Vigushin whose telephone number is 571-272-1936. The examiner can normally be reached on 8:30AM-5:00PM Mo-Fri.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kamand Cuneo can be reached on 571-272-1957. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.


John B. Vigushin
Primary Examiner
Art Unit 2841

jbv
June 19, 2006